

FIG. 1A

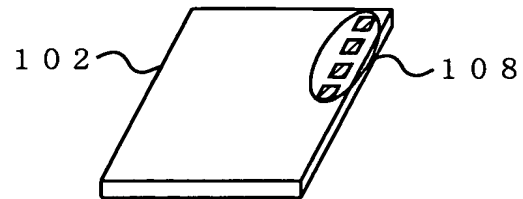


FIG. 1B

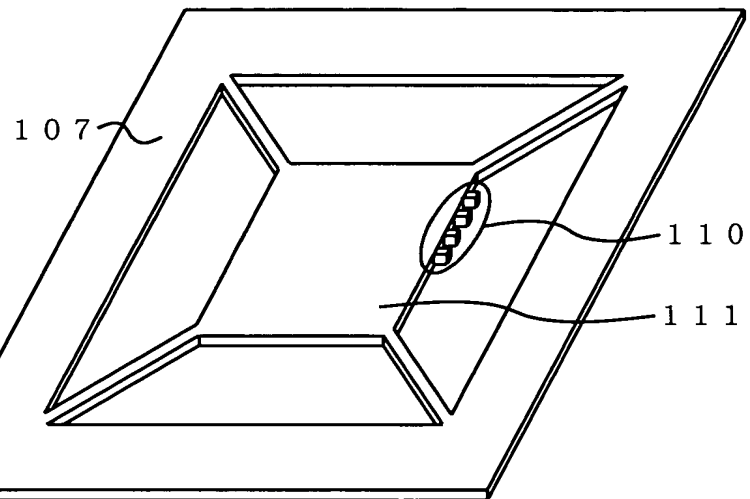


FIG. 1C

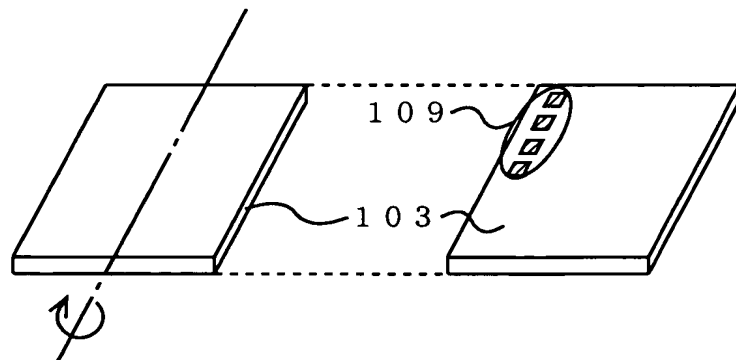


FIG. 2

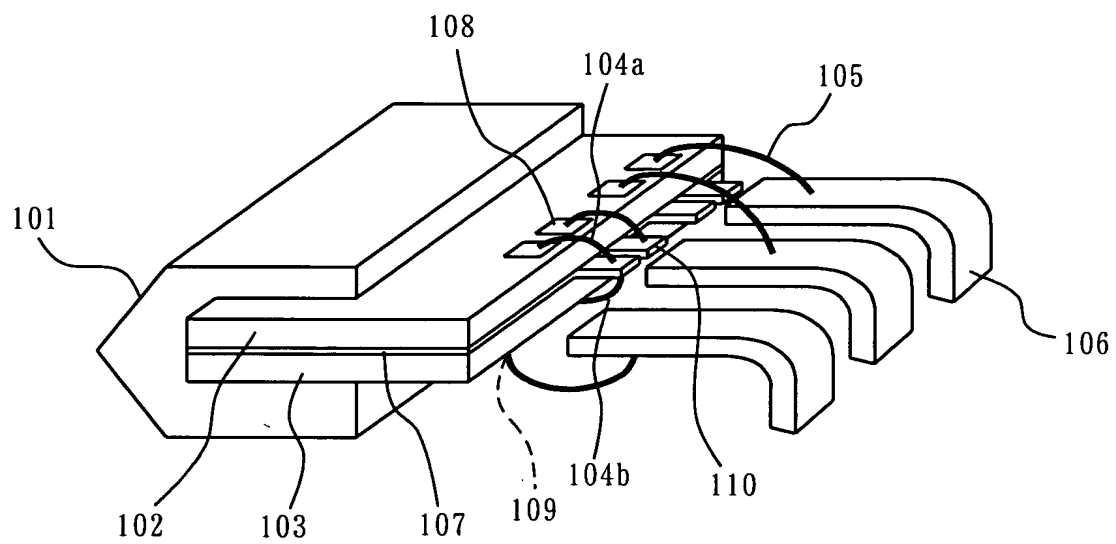


FIG. 3A

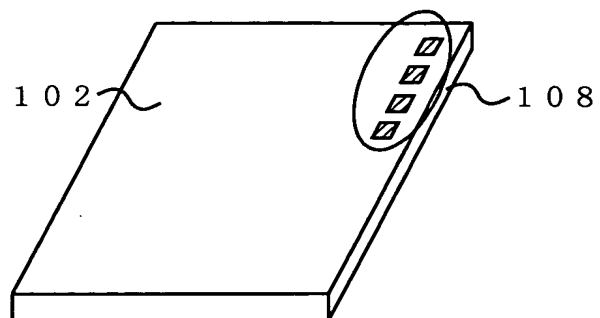


FIG. 3B

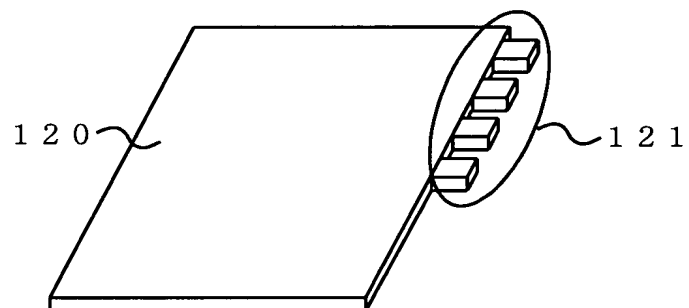


FIG. 3C

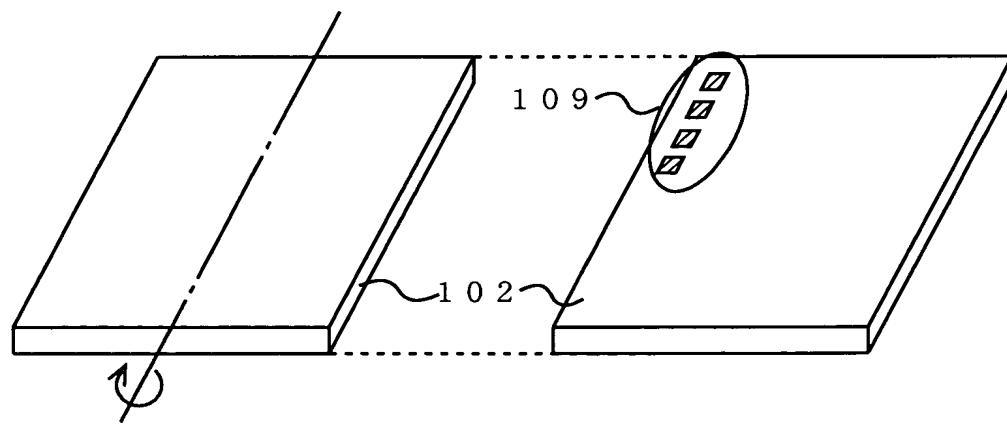


FIG. 4A

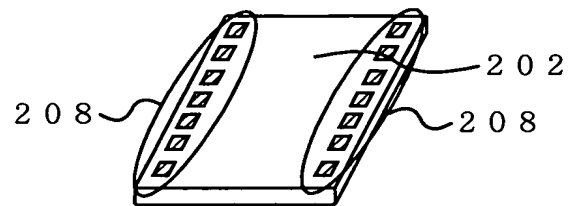


FIG. 4B

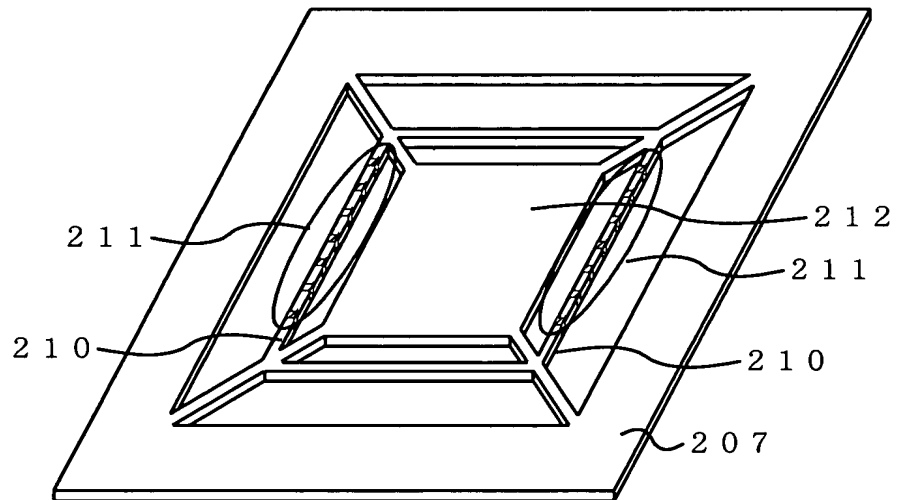
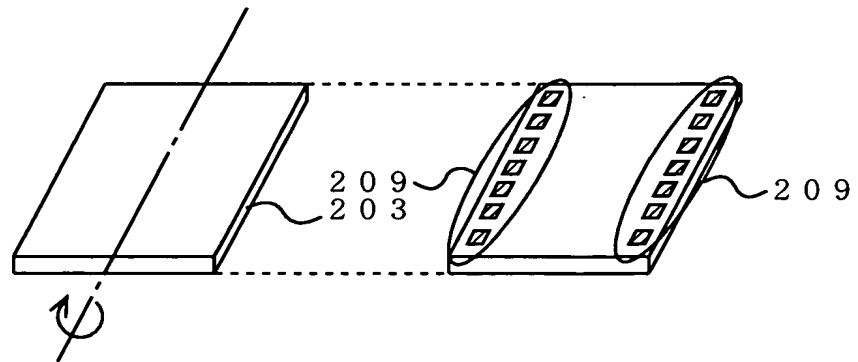


FIG. 4C



This figure shows a perspective view of a multi-layered electronic device assembly. The main body consists of several stacked layers labeled 201, 202, 203, 207, 210, and 211. On the top surface of layer 211, there are two sets of conductive traces or pads labeled 204a and 204b. A series of vertical vias or pillars, labeled 206, connect the top surface to internal layers. A curved arrow indicates a cross-sectional view taken along line 209. Other labels include 208 pointing to a side wall and 205 pointing to a specific feature on the top surface.

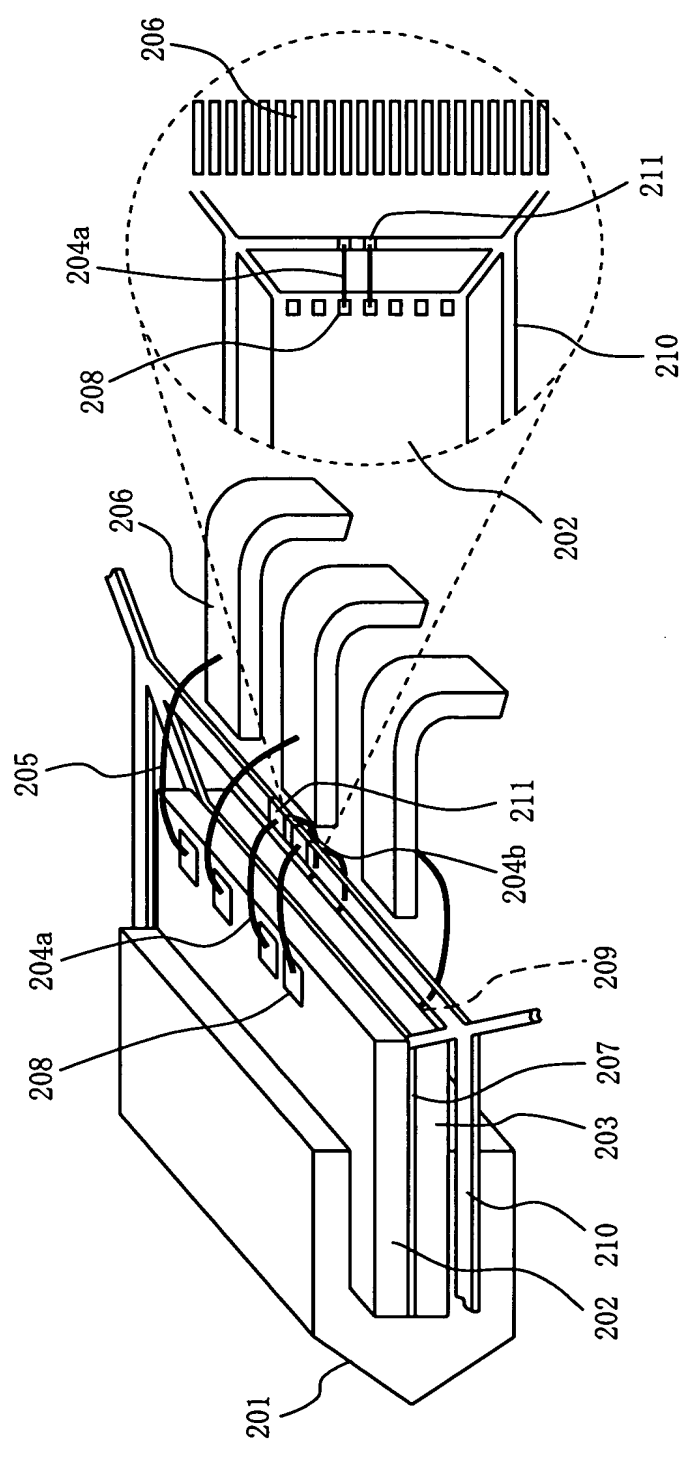


FIG. 6A

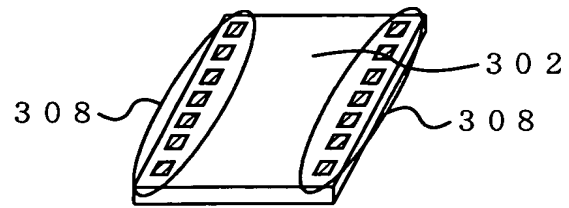


FIG. 6B

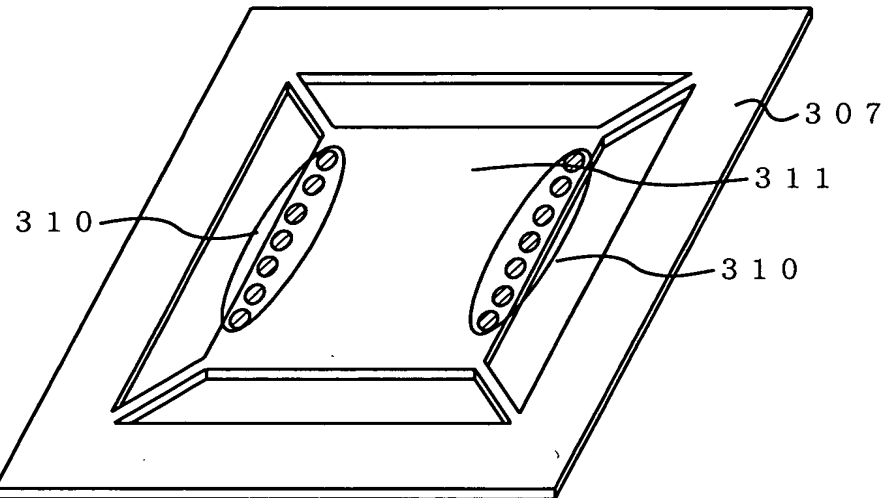


FIG. 6C

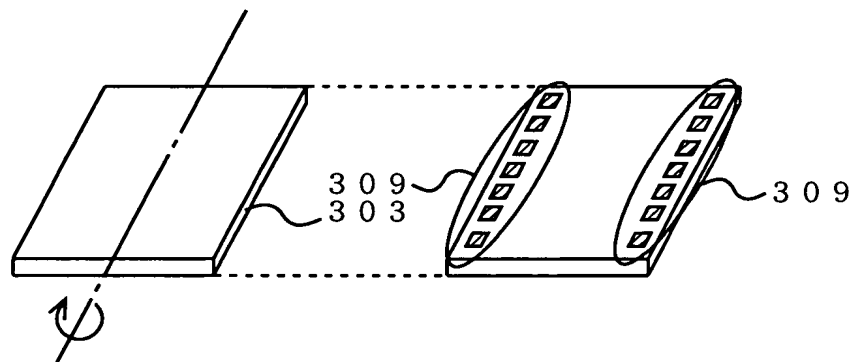


FIG. 7

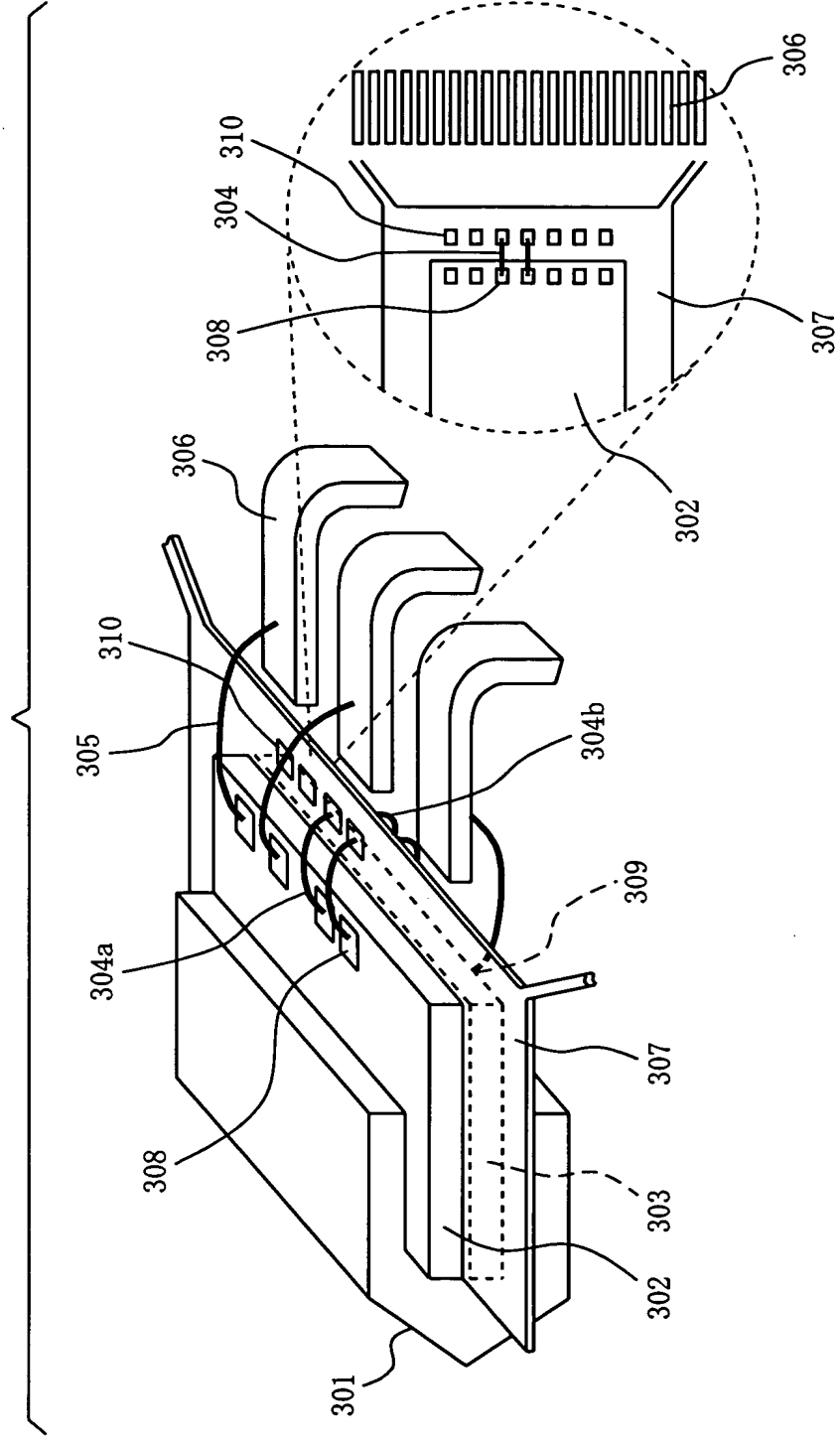


FIG. 8

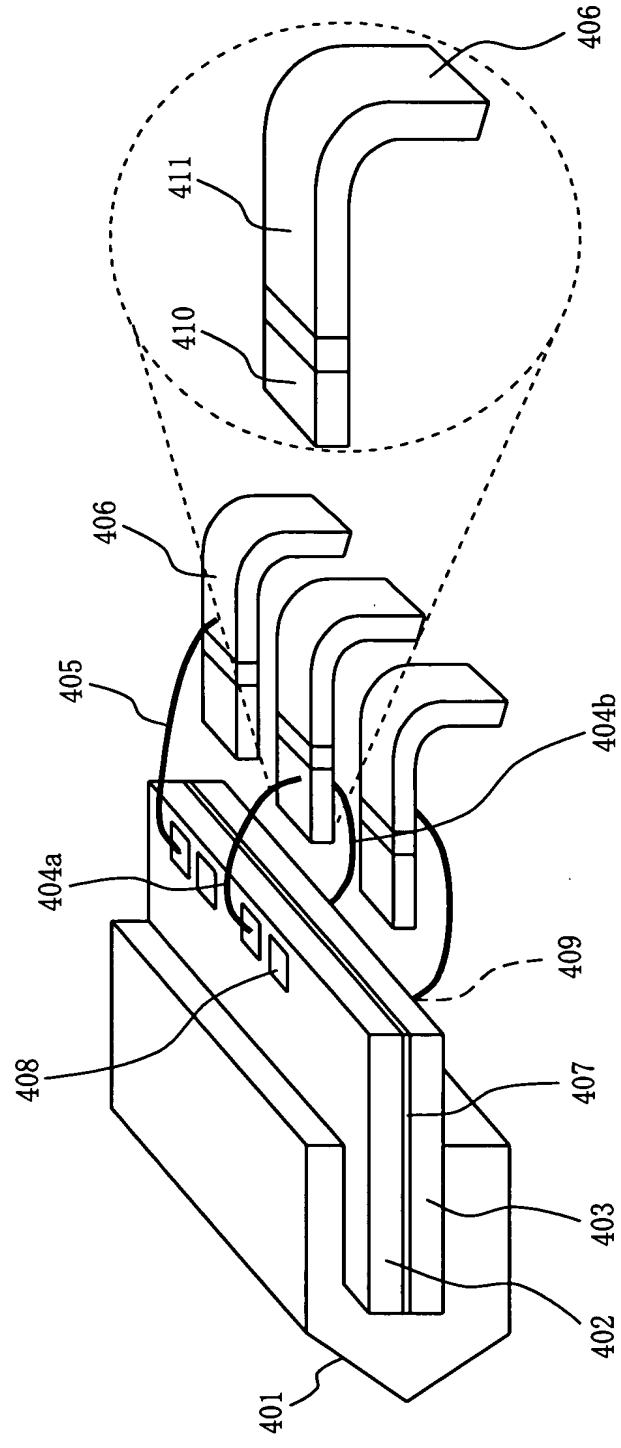




FIG. 9A

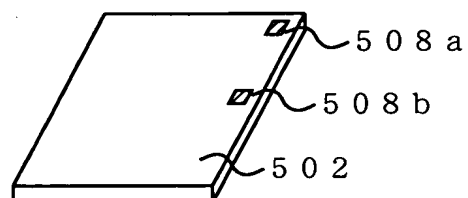


FIG. 9B

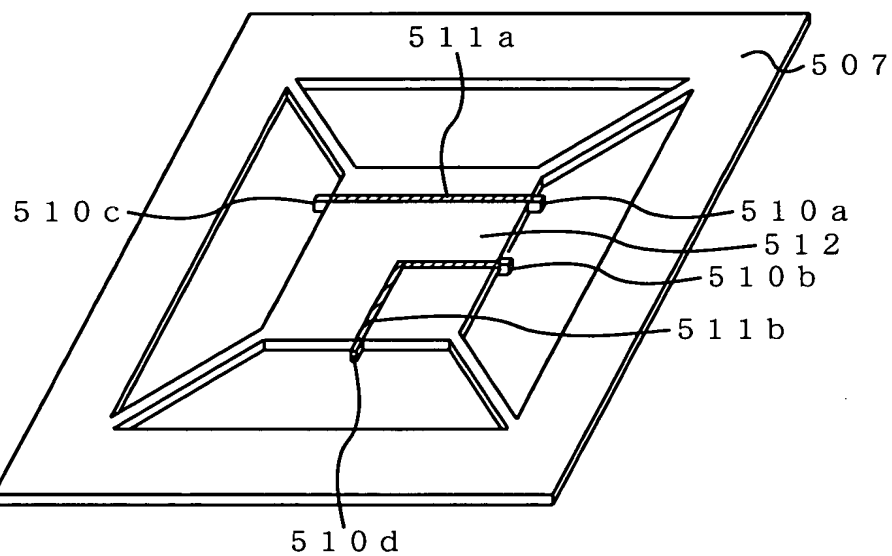


FIG. 9C

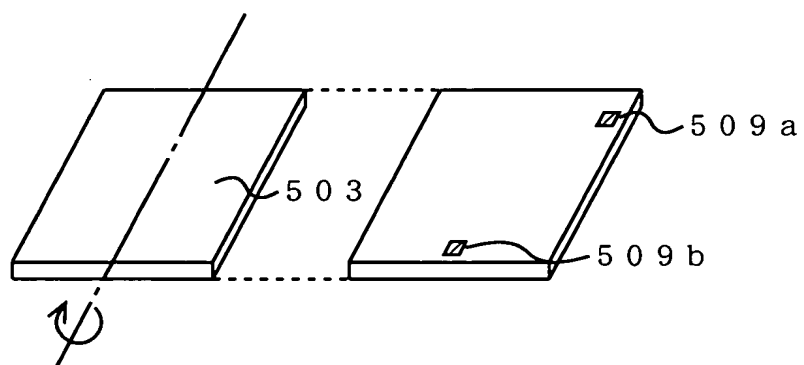


FIG. 10

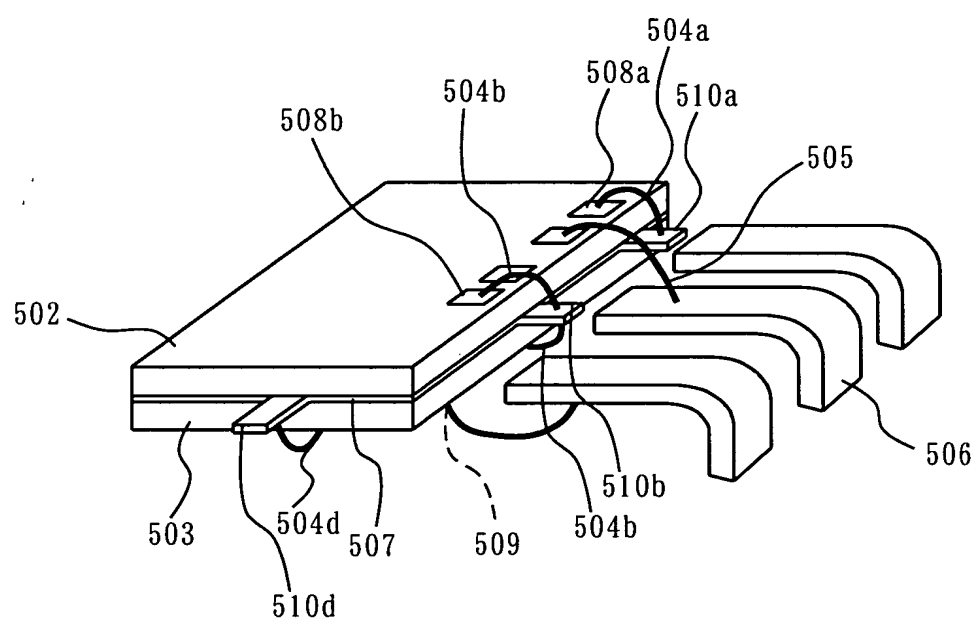


FIG. 11A

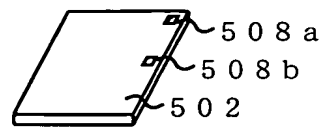


FIG. 11B

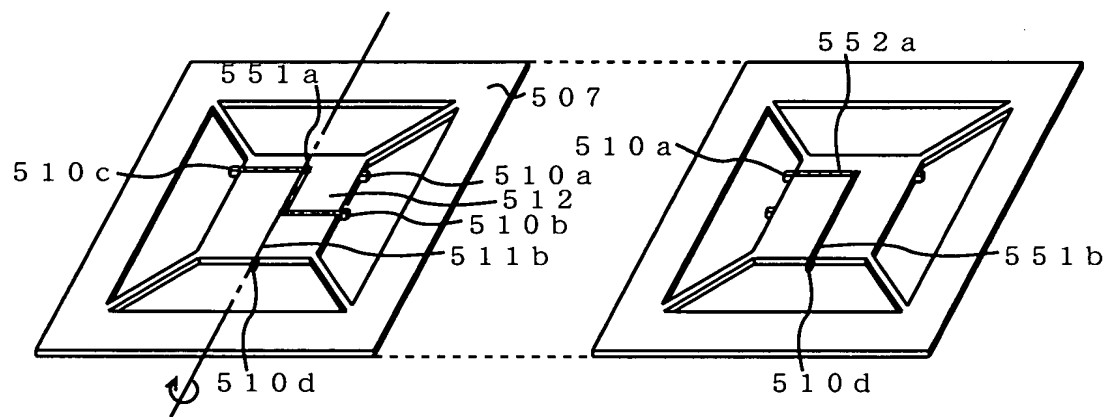


FIG. 11C

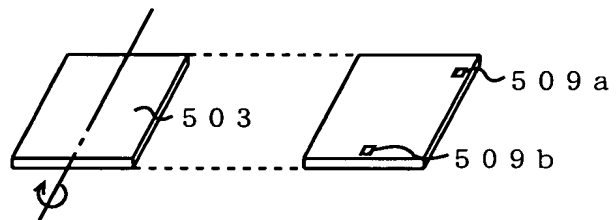


FIG. 12A

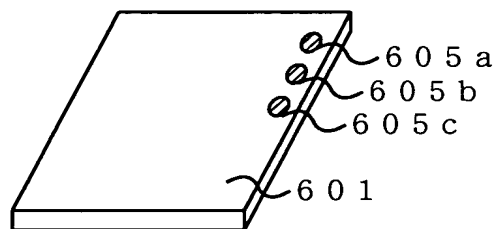


FIG. 12B

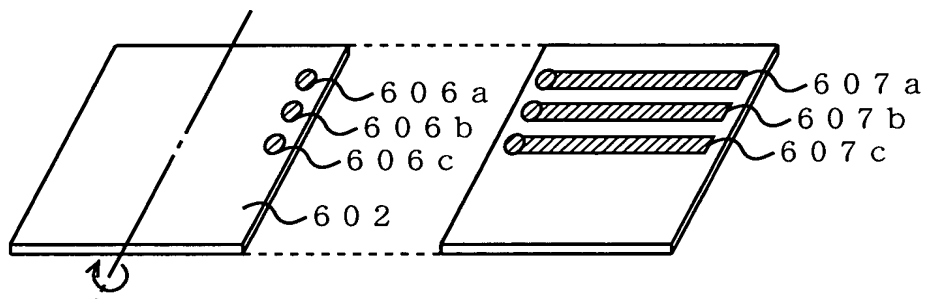
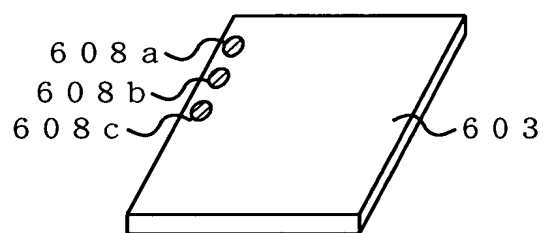


FIG. 12C



F I G. 1 3

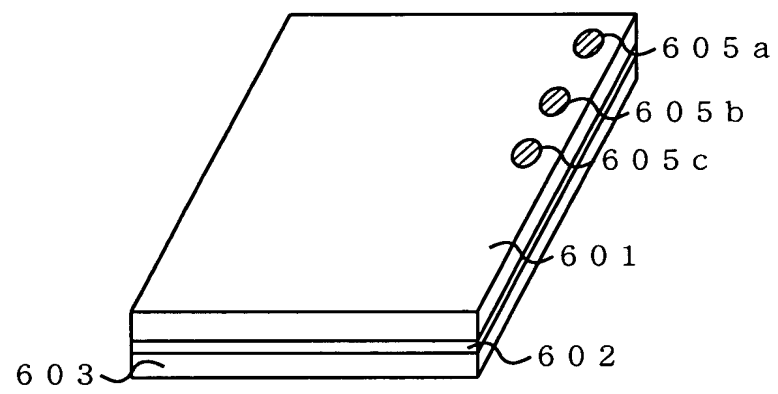


FIG. 14

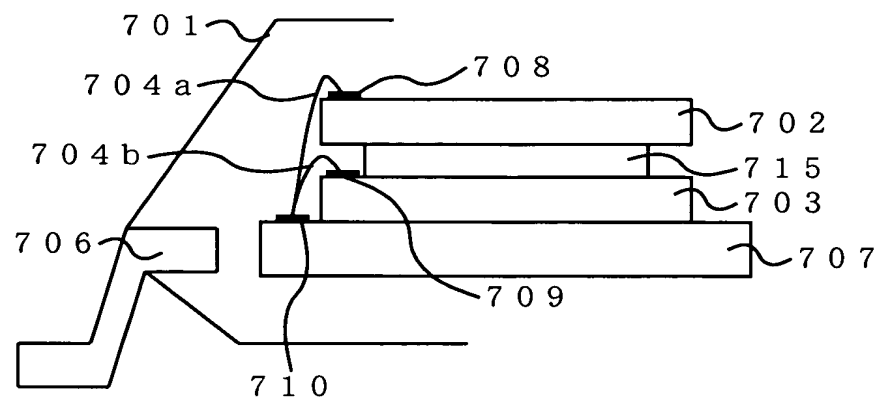


FIG. 15

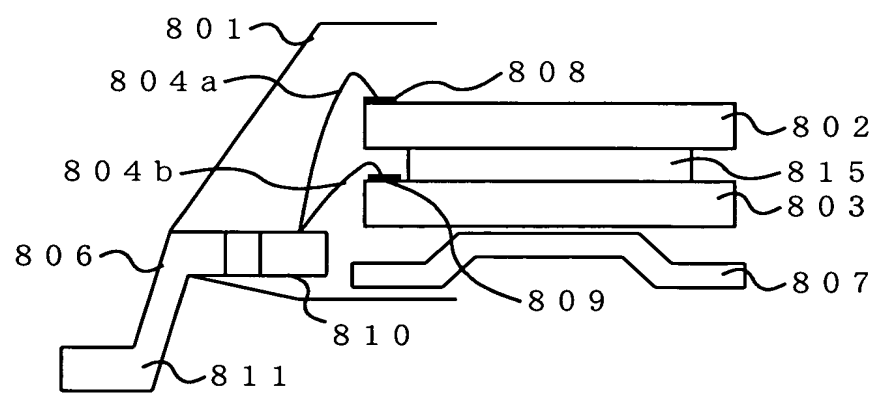


FIG. 16A

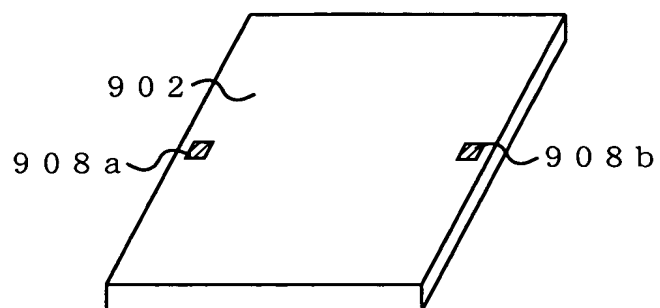


FIG. 16B

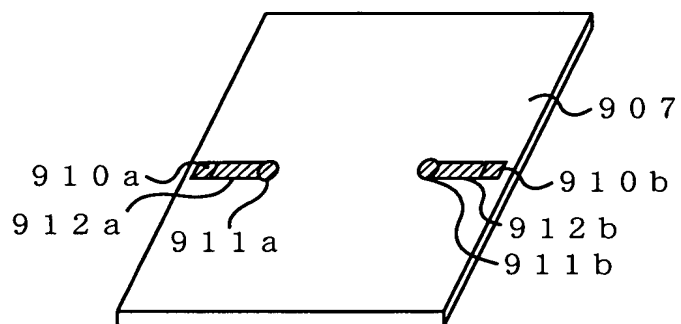


FIG. 16C

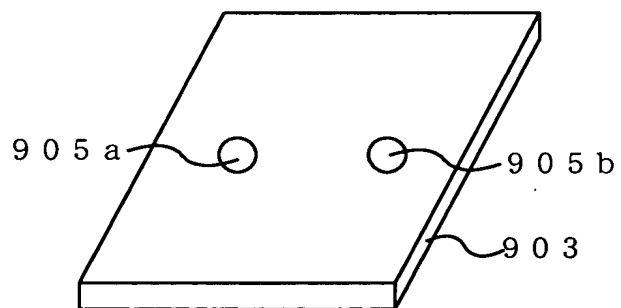


FIG. 17

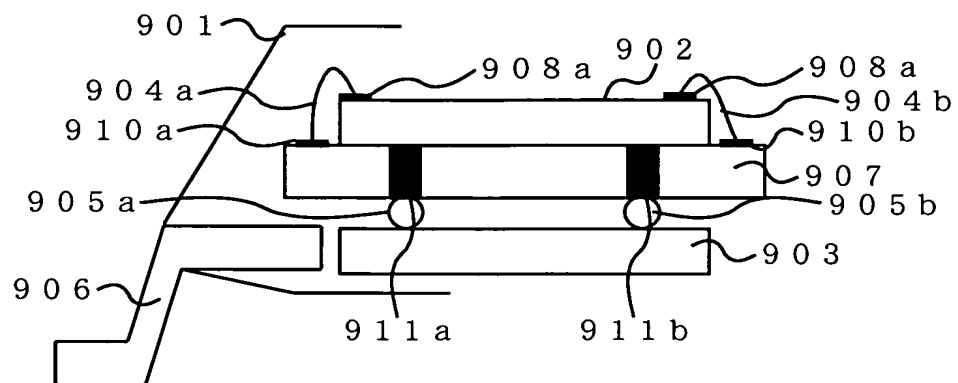


FIG. 18 PRIOR ART

